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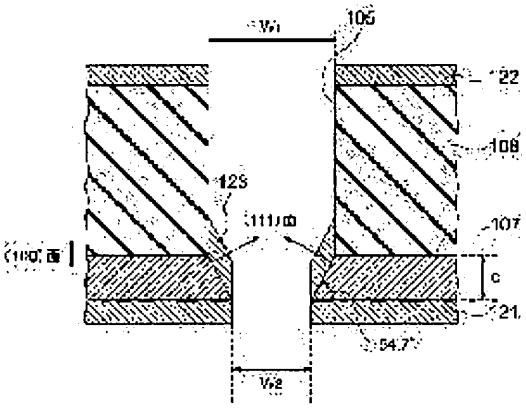
(54) MASK AND ITS PRODUCING METHOD AND METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a mask on which a fine pattern is formed with high accuracy, its producing method and a method for fabricating a semiconductor device.

SOLUTION: The mask comprises a silicon single crystal film 107 having a (100) face in parallel with the surface, a thin film 103 including the silicon single crystal film 107, a hole 105 for passing a charged particle beam, a (111) face defining the wall face of the hole 105 and can delay the etching rate as compared with the (100) face, and conductive layers 121, 122 and 123 for supporting the thin film formed thereon. A method for producing the mask and a method for fabricating a semiconductor device are also provided.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to a stencil mask for electron beam transcription mold lithography and a manufacturing method for the same, and the manufacturing method of a semiconductor device including an electron beam transcription mold lithography process especially about a mask for lithography and a manufacturing method for the same, and the manufacturing method of a semiconductor device.
[0002]
[Description of the Prior Art]Utilization of electron beam transcription mold lithography (EPL;Electron beam Projection Lithography) is expected with the minuteness making of LSI, and high integration. As EPL to which utilization is advanced, PREVAIL (projection exposure with variable axis immersion lenses) (Journal H. C. Pfeiffer others.) which IBM and NIKON are developing jointly ofVacuum Science and Technology B17 p.2840 (1999) are mentioned. RIPURU, LEEPL (lowenergy electron-beam proximity projection lithography) (Journal T. Utsumi) which Tokyo Seimitsu and Sony are developing jointly of Vacuum Science and Technology B17 p.2897 (1999) are mentioned.
[0003]As a mask used for EPL, the stencil mask which has a hole (aperture) in some thin films (membrane), and the membrane mask which has a heavy metal layer in the part on a membrane are proposed. In the case of a stencil mask, an electron beam penetrates an aperture part. In the case of a membrane mask, electron beams are scattered about by a heavy metal layer, and an electron beam penetrates the portion in which the heavy metal layer is not formed.
[0004]Since the electron beam of about 100 keV is used for PREVAIL, both a stencil mask and a membrane mask are available. On the other hand, the electron beam of about 2 keV is used for LEEPL. Since the energy of an electron beam is low, an electron beam does not penetrate

a membrane mask. Therefore, in LEEPL, a stencil mask is used.

[0005]The stencil mask for PREVAIL has an aperture corresponding to a pattern in the silicon membrane of 2-micrometer thickness. PREVAIL(s) are usually 4 times as many reduction projection systems. An electron beam penetrates only an aperture part by no being scattered about, and image formation is carried out on resist. Thereby, exposure is performed to resist by the predetermined pattern.

[0006]The stencil mask for LEEPL has an aperture corresponding to a pattern in the silicon membrane or the diamond membrane of 500-nm thickness. LEEPL is a projection system of actual size. An electron beam penetrates only an aperture part and a pattern is transferred by resist.

[0007]Drawing 18 is a sectional view of the conventional stencil mask. As shown in drawing 18, the stencil mask 201 has the membrane 203 of a predetermined size in the silicon wafer 202. The beam called the strut 204 is formed in the circumference of the membrane 203. The aperture 205 corresponding to a mask pattern is formed in the membrane 203. By forming an aperture in the membrane 203, the mechanical strength of the membrane 203 falls remarkably. The strut 204 acts as a base material for reinforcing the mechanical strength of the stencil mask 201.

[0008]When forming the stencil mask 201 using a silicon wafer, the height of the strut 204 is set to 725 micrometers. The membrane 203 is a part of silicon layer 206, and the surface of the silicon layer 206 is usually a field (100). The silicon oxide 207 is formed between the silicon layer 206 containing the membrane 203 and the strut 204. In the process of etching into the rear face of the silicon wafer 202, and forming the strut 204, the silicon oxide 207 is used as an etching stopper layer.

[0009]In order to manufacture the above stencil masks 201, as shown in drawing 19 (a), the SOI wafer 211 is produced first. The SOI wafer 211 has the silicon layer 206 via the silicon oxide 207 in one field of the silicon wafer 202. The rear-face side silicon oxide 212 is formed in the field of another side of the silicon wafer 202 if needed.

[0010]Next, as shown in drawing 19 (b), the resist 213 is formed in the rear-face side of the SOI wafer 211 by the pattern of a strut. Dry etching is performed to the rear-face side silicon oxide 212 and the silicon wafer 202 from the rear-face side of the SOI wafer 211 by using resist 213 as a mask. Thereby, the strut 204 which consists of silicon is formed.

[0011]When not forming the rear-face side silicon oxide 212, there is a case where the resist 213 is etched and it disappears before etching of the silicon wafer 202 is completed, and it becomes impossible to form a strut. Therefore, the rear-face side silicon oxide 212 is formed as an etching mask.

[0012]Next, as shown in drawing 19 (c), it etches into the silicon oxide 207 by using the strut 204 as a mask. Then, the resist 213 is removed. Next, as shown in drawing 19 (d), the resist

214 of a predetermined pattern is formed on the silicon layer 206. Then, dry etching is performed to the silicon layer 206 by using resist 214 as a mask. Thereby, as shown in drawing 18, the aperture 205 corresponding to a mask pattern is formed in the membrane 203. Then, the stencil mask 201 is obtained by removing the rear-face side silicon oxide 212 and the resist 214.

[0013]As mentioned above, according to the manufacturing method of the conventional stencil mask, an aperture is formed of the dry etching which uses resist as a mask. Dry etching which forms an aperture was performed without taking the crystal face of membrane material into consideration. The sectional shape of the aperture was controlled by adjusting etching conditions, such as a presentation of etching gas, for example.

[0014]

[Problem(s) to be Solved by the Invention]If an aperture is formed in a membrane in accordance with the manufacturing method of the above-mentioned conventional mask, the edge roughness of a resist pattern will be transferred by the mask as it is, and will cause a pattern defect. Since the sectional shape of an aperture changes according to an etching condition, it may not necessarily become vertical sectional shape as shown in drawing 18, a section may serve as tapered shape, or the path of an aperture may become large near the center of a height direction.

[0015]Generally, if minuteness making of the pattern is carried out, the error from a designed size will become large about geometry, such as line width of a mask pattern, and area. Increase of such an error originates, for example in the accuracy of a drawing device, or the characteristic of resist. The section of an aperture serves as tapered shape, and when anticipation of a tapered angle is difficult, the line width of a mask pattern, etc. cannot be controlled with high precision. Therefore, according to the manufacturing method of the above-mentioned conventional mask, it cannot respond to the minuteness making of a future pattern.

[0016]This invention is made in view of the above-mentioned problem, and is a thing.

This invention of the purpose is providing a mask which can form a minute pattern with high precision and a manufacturing method for the same, and the manufacturing method of a semiconductor device.

[0017]

[Means for Solving the Problem]This invention is characterized by a mask comprising the following, in order to attain the above-mentioned purpose.

Single crystal membrane which has the 1st lattice plane in parallel with the surface.

A thin film which contains said single crystal membrane at least.

A hole which was formed in said some of thin films and which a charged particle beam penetrates.

A thin film supporting part formed in a part of 2nd lattice plane that a wall surface of said hole of said single-crystal-membrane portion is constituted, and can make an etch rate late as compared with said 1st lattice plane, and one field of said thin film so that said charged particle beam which penetrated said hole might not be intercepted.

[0018]Suitably, said single crystal membrane is a silicon single crystal film, said 1st lattice plane is a field (100), and said 2nd lattice plane is a field (111). Suitably, said thin film has thin film supporters further on said single crystal membrane. Suitably, said thin film has a thin film support conductive layer further on the surface. Said thin film support conductive layer contains still more suitably the 1st conductive layer formed in a near field in which said thin film supporters of said single crystal membrane are not formed. Suitably, said thin film support conductive layer contains the 2nd conductive layer formed via said thin film supporters on said single crystal membrane. Suitably, said thin film support conductive layer contains the 3rd conductive layer formed in a wall surface of said hole.
[0019]Or suitably, said single crystal membrane is a silicon single crystal film, said 1st lattice plane is a field (110), and said 2nd lattice plane is a field (111). Suitably, said thin film has thin film supporters further on said single crystal membrane. Suitably, said charged particle beam is an electron beam.
[0020]This becomes possible to make a section of a hole flat to an atomic layer order. When a silicon single crystal film which has a field in parallel (100) with the surface is used as single crystal membrane, a tapered angle of a hole can be controlled with high precision at a predetermined angle (54.7 degrees) by making a wall surface of a hole into a field (111). The charge up of a mask at the time of intensity of a thin film being reinforced and performing charged particle beam lithography is prevented by providing a thin film support conductive layer on the surface of a thin film.
[0021]Or when a silicon single crystal film which has a field in parallel (110) with the surface is used as single crystal membrane, sectional shape with a vertical hole is acquired by making a wall surface of a hole into a field (111). Therefore, if lithography is performed using a mask of this invention, roughness of an LSI circuit pattern will be decreased and it will become possible to produce a device with few pattern defects. The endurance of a thin film to stress or heat can be raised by providing thin film supporters.
[0022]In order to attain the above-mentioned purpose, this invention has the 1st single crystal membrane that has the 1st lattice plane in parallel with the surface, and said 1st single crystal membrane formed on said 1st single crystal membrane and the 2nd single crystal membrane from which a crystal axis differs characterized by that a mask of this invention comprises the following.
Said 2nd single crystal membrane that has the 2nd lattice plane in parallel with the surface.

A thin film which contains said 1st single crystal membrane and said 2nd single crystal membrane at least.
A hole which was formed in said some of thin films and which a charged particle beam penetrates.
The 3rd lattice plane that a wall surface of said hole of said 1st single-crystal-membrane portion is constituted, and can make an etch rate late as compared with said 1st lattice plane and said 2nd lattice plane, The 4th lattice plane that a wall surface of said hole of said 2nd single-crystal-membrane portion is constituted, and can make an etch rate late as compared with said 1st lattice plane and said 2nd lattice plane, A thin film supporting part formed in a part of field by the side of the 1st [of said thin film / said] single crystal membrane so that said charged particle beam which penetrated said hole might not be intercepted.

[0023]Suitably, said 1st single crystal membrane is the 1st silicon single crystal film, and said 2nd single crystal membrane is the 2nd silicon single crystal film, Said 1st lattice plane is a field (110), said 2nd lattice plane is a field (100), said 3rd lattice plane is a field (111), and said 4th lattice plane is a field (111). Suitably, said thin film has thin film supporters further on said 2nd silicon single crystal film. Suitably, said charged particle beam is an electron beam.
[0024]This becomes possible to make a section of a hole flat to an atomic layer order. Sectional shape of a hole is controllable with high precision by making a wall surface of a hole into a field (111) using the 2nd silicon single crystal film that has a field in parallel (100) with the surface as the 2nd single crystal membrane using the 1st silicon single crystal film that has a field in parallel (110) with the surface as the 1st single crystal membrane.
[0025]It becomes possible by providing the 2nd silicon single crystal film to form in the 1st silicon single crystal film a pattern to which a pattern of the 2nd silicon single crystal film was reduced. The endurance of a thin film to stress or heat can be raised by providing thin film supporters.
[0026]This invention is characterized by a manufacturing method of a mask comprising the following, in order to attain the above-mentioned purpose.
A process of forming single crystal membrane which has the 1st lattice plane in parallel with the surface on one field of a substrate.
A process of removing said some of substrates from the field side of another side of said substrate, and forming a thin film supporting part.
A process of forming in said single crystal membrane said hole whose wall surface it is a hole which a charged particle beam penetrates by etching into said single crystal membrane on conditions into which said 1st lattice plane is selectively etched to the 2nd lattice plane, and is said 2nd lattice plane.

[0027]Suitably, a manufacturing method of a mask of this invention has further a process of forming thin film supporters on said single crystal membrane, and the process of etching into said thin film supporters on the aforementioned hole before forming said hole in said single crystal membrane, after forming said single crystal membrane. Suitably, said single crystal membrane is a silicon single crystal film, said 1st lattice plane is a field (100), and said 2nd lattice plane is a field (111).

[0028]Suitably, after forming said hole, it has further the process of forming a thin film support conductive layer in said single crystal membrane and at least one surface of said thin film supporters. Suitably, a process of forming said thin film support conductive layer includes physical vacuum evaporation (PVD). Suitably, a process of forming said thin film support conductive layer includes a process of forming the 1st conductive layer in a near field in which said thin film supporters of said single crystal membrane are not formed. Suitably, a process of forming said thin film support metallic layer includes a process of forming the 2nd conductive layer on said thin film supporters. Suitably, a process of forming said thin film support metallic layer includes a process of forming the 3rd conductive layer in a wall surface of said hole.

[0029]Or suitably, said single crystal membrane is a silicon single crystal film, said 1st lattice plane is a field (110), and said 2nd lattice plane is a field (111). In a process in which a manufacturing method of a mask of this invention forms said single crystal membrane suitably, A process of forming said single crystal membrane via an etching stopper layer from which said single crystal membrane and an etch rate differ, and forming said thin film supporting part on said substrate includes a process of etching into said substrate until said etching stopper layer is exposed.

[0030]Thereby, a section of a hole is made flat to an atomic layer order, and it becomes possible to use a section of a hole as a vertical or fixed tapered angle. According to the manufacturing method of a mask of this invention, also when a hole is formed by wet etching, sectional shape with a good hole is acquired.

[0031]Generally, as compared with dry etching, device of wet etching etc. are simple, and if a hole is formed by wet etching, it is possible to reduce a manufacturing cost of a mask. Since breakage of a mask in a mask manufacture process is prevented by providing thin film supporters, a yield of a mask can be raised.

[0032]This invention in order to attain the above-mentioned purpose a manufacturing method of a mask of this invention, Said 1st single crystal membrane and the 2nd single crystal membrane from which a crystal axis differs are characterized by comprising the following on a process of forming the 1st single crystal membrane that has the 1st lattice plane in parallel with the surface on one field of a substrate, and said 1st single crystal membrane:

A process of forming said 2nd single crystal membrane that has the 2nd lattice plane in parallel with the surface.

A process of removing said some of substrates from the field side of another side of said substrate, and forming a thin film supporting part.
When said 2nd lattice plane etches into said 2nd single crystal membrane on conditions selectively etched to the 3rd lattice plane that is one lattice plane of everything but said 2nd single crystal membrane, A process of forming in said 2nd single crystal membrane the 1st opening whose wall surface it is a part of hole which a charged particle beam penetrates, and is the 3rd lattice plane.
When said 1st lattice plane etches into said 1st single crystal membrane on conditions selectively etched to the 4th lattice plane that is one lattice plane of everything but said 1st single crystal membrane, A process of forming in said 1st single crystal membrane the 2nd opening whose wall surface it is said a part of other holes, and is the 4th lattice plane.

[0033]Suitably, a manufacturing method of a mask of this invention has further a process of forming thin film supporters on said 2nd single crystal membrane, and the process of etching into said thin film supporters on said 1st opening before forming said 1st opening in said 2nd single crystal membrane, after forming said 2nd single crystal membrane.
[0034]A manufacturing method of a mask of this invention is provided with the following.
A process of pasting together to said substrate suitably the 2nd substrate with which a process of forming said 2nd single crystal membrane has said 2nd single crystal membrane on the surface so that said 1st single crystal membrane and said 2nd single crystal membrane may touch.
A process of leaving said 2nd single crystal membrane on said 1st single crystal membrane, and removing said 2nd substrate.

[0035]A manufacturing method of a mask of this invention is provided with the following.
A process of grinding said 2nd substrate until said sacrificial film exposes a process of having further the process of forming a sacrificial film between layers of said 2nd substrate and said 2nd single crystal membrane, and removing said 2nd substrate still more suitably before pasting said 2nd substrate together to said substrate.
A process of removing said sacrificial film by etching.

[0036]Suitably, said 1st single crystal membrane is the 1st silicon single crystal film, and said 2nd single crystal membrane is the 2nd silicon single crystal film, Said 1st lattice plane is a field (110), said 2nd lattice plane is a field (100), said 3rd lattice plane is a field (111), and said 4th lattice plane is a field (111).
[0037]In a process in which a manufacturing method of a mask of this invention forms said 1st single crystal membrane suitably, A process of forming said 1st single crystal membrane via

an etching stopper layer from which said 1st single crystal membrane and an etch rate differ, and forming said thin film supporting part on said substrate includes a process of etching into said substrate until said etching stopper layer is exposed.

[0038]Thereby, a section of an aperture is made flat to an atomic layer order, and it becomes possible to use a section of an aperture as a vertical or fixed tapered angle. According to the manufacturing method of a mask of this invention, also when an aperture is formed by wet etching, sectional shape with a good aperture is acquired.

[0039]According to the manufacturing method of a mask of this invention, by laminating single crystal membrane from which a crystal axis differs, a pattern formed in the upper single crystal membrane (the 2nd single crystal membrane) can be reduced, and it can form in lower layer single crystal membrane (the 1st single crystal membrane). Since breakage of a mask in a mask manufacture process is prevented by providing thin film supporters, a yield of a mask can be raised.

[0040]Furthermore, this invention in order to attain the above-mentioned purpose a manufacturing method of a semiconductor device of this invention, Via a mask in which a predetermined mask pattern was formed, it irradiates with a charged particle beam on a substrate, and a manufacturing method of a semiconductor device which has the process of transferring said mask pattern to said substrate is characterized by comprising the following:

Single crystal membrane which has the 1st lattice plane in parallel with the surface as for said mask.

A thin film which contains said single crystal membrane at least.

A hole which was formed in said some of thin films and which a charged particle beam penetrates.

A thin film supporting part formed in a part of 2nd lattice plane that a wall surface of said hole of said single-crystal-membrane portion is constituted, and can make an etch rate late as compared with said 1st lattice plane, and one field of said thin film so that said charged particle beam which penetrated said hole might not be intercepted.

[0041]Suitably, said single crystal membrane is a silicon single crystal film, said 1st lattice plane is a field (100), and said 2nd lattice plane is a field (111). Or suitably, said single crystal membrane is a silicon single crystal film, said 1st lattice plane is a field (110), and said 2nd lattice plane is a field (111).

[0042]This invention irradiates with a charged particle beam on a substrate via a mask in which a predetermined mask pattern was formed, and a manufacturing method of a semiconductor device of this invention is characterized by that a manufacturing method of a semiconductor device which has the process of transferring said mask pattern to said substrate comprises the following.

The 1st single crystal membrane that has the 1st lattice plane in parallel with the surface as for said mask.
Said 2nd single crystal membrane that is said 1st single crystal membrane formed on said 1st single crystal membrane, and the 2nd single crystal membrane from which a crystal axis differs, and has the 2nd lattice plane in parallel with the surface.
A thin film which contains said 1st single crystal membrane and said 2nd single crystal membrane at least.
A wall surface of a hole which was formed in said some of thin films and which a charged particle beam penetrates, and said hole of said 1st single-crystal-membrane portion is constituted, The 3rd lattice plane that can make an etch rate late as compared with said 1st lattice plane and said 2nd lattice plane, The 4th lattice plane that a wall surface of said hole of said 2nd single-crystal-membrane portion is constituted, and can make an etch rate late as compared with said 1st lattice plane and said 2nd lattice plane, A thin film supporting part formed in a part of field by the side of the 1st [of said thin film / said] single crystal membrane so that said charged particle beam which penetrated said hole might not be intercepted.

[0043]Suitably, said 1st single crystal membrane is the 1st silicon single crystal film, and said 2nd single crystal membrane is the 2nd silicon single crystal film, Said 1st lattice plane is a field (110), said 2nd lattice plane is a field (100), said 3rd lattice plane is a field (111), and said 4th lattice plane is a field (111).
[0044]Thereby, roughness of an LSI circuit pattern is decreased and it becomes possible to produce a device with few pattern defects. It becomes possible to form a pattern by which minuteness making was carried out to an LSI circuit with high precision.
[0045]
[Embodiment of the Invention]Below, the embodiment of a mask of this invention, and the manufacturing method and the manufacturing method of a semiconductor device for the same is described with reference to drawings.
(Embodiment 1) Drawing 1 is a sectional view of the mask of this embodiment, and drawing 2 is the figure to which the hole (aperture) portion of drawing 1 was expanded. The stencil mask of this embodiment is used suitably for LEEPL which is one of the EPL(s).
[0046]As shown in drawing 1, the stencil mask 101 of this embodiment has the membrane 103 of a predetermined size on the silicon wafer 102. In the case of this embodiment, the size of the membrane 103 is used for example, as 25 mm squares. The strut 104 is formed in the circumference of the membrane 103. The aperture 105 corresponding to a mask pattern is formed in the membrane 103. The mechanical strength of the membrane 103 falls by forming an aperture in the membrane 103. The strut 104 acts as a base material for reinforcing the mechanical strength of the stencil mask 101.

[0047]According to the stencil mask 101 of this embodiment, the membrane 103 consists of the silicon layer 107, the silicon nitride film 108, the 1st metal layer 121, the 2nd metal layer 122, and the 3rd metal layer 123. The silicon nitride film 108 is formed on the silicon layer 107. The 1st metal layer 121 is formed in the near field in which the silicon nitride film 108 of the silicon layer 107 is not formed. The 2nd metal layer 122 is formed on the silicon nitride film 108. The 3rd metal layer 123 is formed in aperture 105 wall surface of silicon layer 107 portion at least.

[0048]The silicon nitride film 108 and the 1st - the 3rd metal layer 121, 122, and 123 are formed as membrane supporters for raising the mechanical strength of the membrane 103. The position of the entering electron can be prevented from the stencil mask 101 being charged when performing EPL (charge up), and shifting by forming the 1st - the 3rd metal layer 121, 122, and 123. As long as reinforcement of the membrane 103 and prevention of the charge up are possible, the conductive layer which consists of materials other than metal may be formed instead of the 1st - the 3rd metal layer 121, 122, and 123.

[0049]It is not necessary to necessarily form altogether the 1st - the 3rd metal layer 121, 122, and 123. When the 3rd metal layer 123 is not formed by uniform thickness, the edge roughness of a mask pattern poses a problem. Usually, the 3rd metal layer 123 may form only the 1st metal layer 121, in order to avoid increase of such edge roughness, since it is formed at the same process as the 2nd metal layer 122.

[0050]As shown in drawing 1, the silicon oxide 109 is formed between the silicon layer 107 containing the membrane 103 and the strut 104. In the process of etching into the rear face of the silicon wafer 102, and forming the strut 104, the silicon oxide 109 is used as an etching stopper layer.

[0051]As shown in drawing 2, in the interface of the silicon layer 107 and the silicon nitride film 108, the surface of the silicon layer 107 is a field (100). The section of the silicon layer 107 to the aperture 105 is a field (111). According to the stencil mask of this embodiment, the aperture 105 is formed in consideration of the crystal face orientation of membrane material. The angle of the interface of the silicon layer 107 and the 1st metal layer 121 and the field which is sections of the silicon layer 107 (111) to make is 54.7 degrees.

[0052]Thus, since the tapered angle of the aperture 105 is controlled using the crystal face orientation of membrane material, a tapered angle can be made regularity also when minuteness making of the pattern is carried out further. Line width W_2 of a mask pattern is determined by thickness [of line width W_1 of silicon nitride film 108 portion, and the silicon layer 107] d, and the tapered angle.

[0053]If the resist of line width W_1 can be formed also when resist of line width W_2 cannot be formed on the silicon nitride film 108 according to the mask of this embodiment shown in

drawing 2, A mask pattern can be formed by line width W_2 reduced rather than line width W_1. Here, since the tapered angle of an aperture is constant, line width W_1 is reduced with high precision.

[0054]Next, the manufacturing method of the stencil mask of this embodiment is explained. In order to manufacture the stencil mask of this embodiment, as shown in drawing 3 (a), the surface forms the silicon nitride film 108 in the surface of the SOI wafer 124 which is a field (100) as membrane supporters first.

[0055]The SOI wafer 124 has the silicon layer 107 via the silicon oxide 109 on the silicon wafer 102. The thickness of the silicon wafer 102 is 725 micrometers. The thickness of the silicon oxide 109 is 100 nm. The thickness of the silicon layer 107 is 50 nm. The thickness of the silicon layer 107 may be suitably changed according to the energy of the electron beam at the time of performing EPL using a stencil mask, and the line width converted quantity (W_1-W_2) of an aperture. The surface of the silicon layer 107 is a field (100).

[0056]The silicon nitride film 108 is formed with chemical vapor deposition (CVD;chemical vapor deposition). The thickness of the silicon nitride film 108 shall be 500 nm. If membrane supporters are the material which is not etched by etchant at the time of etching into the silicon layer 107, and can support the membrane of the size (for example, 25 mm squares) corresponding to a chip area, they can also change into other materials.

[0057]As etchant for silicon layer 107, for example, when a potassium hydrate (KOH) or tetramethylammonium hydroxide (TMAH;tetramethylammoniumhydroxide) is used, Layers, such as silicon oxide, a silicon oxidation nitride, a diamond, DLC (diamond like carbon), and metal, may be formed by a thickness of about 100-3000 nm instead of a silicon nitride film.

[0058]Next, as shown in drawing 3 (b), the resist 118 is formed on the silicon nitride film 108. Interval W_1 of the resist 118 is made larger than line width W_2 of the lower end of the silicon layer 107 shown in drawing 2. Then, the pattern of the resist 118 is transferred by the silicon nitride film 108 by etching into the silicon nitride film 108 by using resist 118 as a mask. Let this etching be the dry etching which used CF_4 etc., for example. Then, the resist 118 is removed.

[0059]Next, as shown in drawing 3 (c), wet etching is performed to the silicon layer 107 by using the silicon nitride film 108 as a mask. For example, when a wafer is immersed in a KOH solution with a temperature of 70 ** concentration 30wt%, the etching rate of field (111) silicon is extremely as late as a part for 5-nm/to the etching rate of field (100) silicon being 797/.

[0060]That is, in the perpendicular direction of the silicon layer 107, etching hardly advances with about 108 silicon nitride film to etching advancing promptly. Therefore, the etching section in the silicon layer 107 serves as tapered shape equivalent to a field (111), and this (111) field makes the angle of 54.7 degrees to the field (100) of the silicon layer 107 (refer to drawing 2).

[0061]As a result, line width W_2 in the lower end of the silicon layer 107 becomes narrower than line width W_1 of the resist 118 or the silicon nitride film 108. When thickness of the silicon layer 107 is set to d, it is expressed $W_2=W_1-2$ d/tan54.7" and line width W_1 is reduced to line width W_2 according to thickness d of the silicon layer 107.

[0062]In this embodiment, a W_2=35nm detailed pattern is formed with high precision from thickness d of the silicon layer 107 being 50 nm by line width W_1 of the resist 118 or the silicon nitride film 108 being 105.8 nm, for example. When an aperture is formed as mentioned above using the difference in the etching rate by a crystal face, sectional shape of an aperture can be made flat to an atomic layer order, or an aperture can be processed with the sectional shape of a predetermined tapered angle.

[0063]Even if it uses a TMAH solution for etchant when performing wet etching to the silicon layer 107, an etching rate changes according to a crystal face. For example, when a wafer is immersed in a TMAH solution with a temperature of 80 ** concentration 20wt%, the etching rate of silicon becomes in a field (100), and becomes a part for 17-nm/by 603-nm/in a field (111). Therefore, like the case where a KOH solution is used, it can etch into a specific crystal face selectively, and the surface smoothness and shape of an aperture section can be controlled with high precision.

[0064]Next, as shown in drawing 4 (d), it etches into the silicon wafer 102 by using resist (un-illustrating) as a mask from the rear-face side, and the strut 104 is formed. Although it is not necessary to necessarily form the rear-face side silicon oxide 116, when dry etching is performed without forming the rear-face side silicon oxide 116, there is a case where resist is etched and it disappears before etching of the silicon wafer 102 is completed, and it becomes impossible to form a strut. Therefore, the rear-face side silicon oxide 116 is formed as an etching mask.

[0065]Next, as shown in drawing 4 (e), the silicon oxide 109 of membrane 103 portion is removed. The silicon oxide 109 is removable by the wet etching which used fluoric acid, for example. The rear-face side silicon oxide 116 is also removed by this wet etching.

[0066]Next, as shown in drawing 4 (f), PVD(s), such as a sputtering technique and a vacuum deposition method, are carried out to one field of a mask, and the 2nd metal layer 122 and 3rd metal layer 123 are formed in it. As a material of the 2nd and 3rd metal layers 122 and 123, metal, such as platinum, palladium, gold, aluminum, titanium, molybdenum, chromium, iridium, and tungsten, is used, for example. These metal layers may not be formed but the conductive layer which consists of materials other than metal may be formed by PVD.

[0067]According to the energy of the electron beam at the time of performing EPL using a stencil mask, the intensity of the silicon layer 107 sets up the thickness of the 2nd and 3rd

metal layers 122 and 123 in the range fully reinforced. The thickness of the 2nd and 3rd metal layers 122 and 123 shall be about 5-200 nm, for example. In LEEPL which sets accelerating voltage of an electron beam to 2keV, it is desirable for the thickness of the 2nd metal layer 122 to be about 20-30 nm.

[0068]Then, as shown in drawing 1, PVD is performed like the field of another side of a mask, and the 1st metal layer 121 is formed. As a material of the 1st metal layer 121, the same metal as the 2nd and 3rd metal layers 122 and 123 can be used. The thickness of the 1st metal layer 121 is set up like the 2nd and 3rd metal layers 122 and 123. However, the thickness of the 2nd and 3rd metal layers 122 and 123 may differ from the thickness of the 1st metal layer 121.

[0069]By the above process, the stencil mask 101 shown in drawing 1 is obtained. According to the manufacturing method of the mask of this above-mentioned embodiment, after etching into the silicon nitride film 108 and the silicon layer 107 and forming the aperture 105, it etches into the silicon wafer 102 and the strut 104 is formed. However, after etching into the silicon wafer 102 and forming the strut 104 like Embodiment 1, it can also etch into the silicon nitride film 108 and the silicon layer 107.

[0070]The manufacturing method of the semiconductor device of this embodiment includes the process of producing a stencil mask in accordance with the manufacturing method of the mask of this above-mentioned embodiment, and performing LEEPL using the produced mask. Since a minute pattern performs EPL using the mask formed with high precision according to the manufacturing method of the semiconductor device of this embodiment, the pattern defect of an LSI pattern can be reduced.

[0071](Embodiment 2) Drawing 5 is a sectional view of the mask of this embodiment. As shown in drawing 5, the stencil mask 131 of this embodiment has the stencil mask 101 of Embodiment 1, and a common structure except for the shape of the strut 104. Therefore, the composition of the membrane 103 and the structure of an aperture part are the same as that of drawing 2.

[0072]As for the stencil mask 131 of this embodiment, the strut 104 is formed of wet etching. In this case, if an aperture is formed in the silicon nitride film 108 and the silicon layer 107 before forming the strut 104, when forming the strut 104, it will be necessary to protect the silicon layer 107 of an aperture part. Therefore, when forming the strut 104 by wet etching, before forming the aperture 105, it is desirable to form the strut 104.

[0073]Hereafter, the manufacturing method of the stencil mask of this embodiment is explained. In order to manufacture the stencil mask 131 of this embodiment, as shown in drawing 6 (a), the surface forms the silicon nitride film 108 in the surface of the SOI wafer 124 which is a field (100) as membrane supporters first like the process shown in drawing 3 (a) of Embodiment 1.

[0074]Next, as shown in drawing 6 (b), resist is formed in the rear face of the silicon wafer 102

by the pattern of a strut. Wet etching is performed to the silicon wafer 102 by using resist as a mask. Thereby, the strut 104 is formed. KOH, TMAH, etc. are used for this wet etching as etchant. In this etching, the silicon oxide 109 serves as an etching stopper layer. Resist is removed after etching.

[0075]Next, like the process shown in drawing 3 (b) and (c) of Embodiment 1, as shown in drawing 6 (c), it etches into the silicon nitride film 108 and the silicon layer 107. Dry etching which uses resist (un-illustrating) as a mask is performed in the silicon nitride film 108.

[0076]On the other hand, wet etching is performed by using the silicon nitride film 108 as a mask at the silicon layer 107. KOH, TMAH, etc. are used for this wet etching as etchant. It is possible to make sectional shape of an aperture flat to an atomic layer order, or to control the tapered angle of a section with high precision by this.

[0077]Next, the silicon oxide 109 of membrane 103 portion is removed like the process shown in drawing 4 (e) of Embodiment 1. Then, the 2nd and 3rd metal layers 122 and 123 are formed in one field of a mask like the process shown in drawing 4 (f) of Embodiment 1. The stencil mask 131 shown in drawing 5 is obtained by forming the 1st metal layer 121 in the field of another side of a mask.

[0078](Embodiment 3) Drawing 7 is a sectional view of the mask of this embodiment, and drawing 8 is the figure to which the aperture part of drawing 7 was expanded. The stencil mask of this embodiment is used suitably for LEEPL which is one of the EPL(s).

[0079]As shown in drawing 7, the stencil mask 141 of this embodiment has the membrane 103 of a predetermined size on the silicon wafer 102. In the case of this embodiment, the size of the membrane 103 is used for example, as 25 mm squares. The strut 104 is formed in the circumference of the membrane 103. The aperture 105 corresponding to a mask pattern is formed in the membrane 103. The mechanical strength of the membrane 103 falls by forming an aperture in the membrane 103. The strut 104 acts as a base material for reinforcing the mechanical strength of the stencil mask 141.

[0080]According to the stencil mask 141 of this embodiment, the membrane 103 consists of three layers of the silicon layer 106, the silicon layer 107 formed on the silicon layer 106, and the silicon nitride film 108 formed on the silicon layer 107. The silicon nitride film 108 is formed as membrane supporters for raising the mechanical strength of the membrane 103. Although not illustrated, conductivity is given to the silicon layer 106, an impurity may be doped to the silicon layer 106, or a conductive layer may be formed in the silicon layer 106 surface in order to prevent the charge up of the stencil mask 141.

[0081]As shown in drawing 7, the silicon oxide 109 is formed between the silicon layer 106 containing the membrane 103 and the strut 104. In the process of etching into the rear face of the silicon wafer 102, and forming the strut 104, the silicon oxide 109 is used as an etching stopper layer.

[0082]As shown in drawing 8, in the interface of the silicon layer 106 and the silicon layer 107, the surface of the silicon layer 106 is a field (110). In the interface of the silicon layer 107 and the silicon nitride film 108, the surface of the silicon layer 107 is a field (100). The surface of the silicon layer 106 exposed in the aperture 105 is a field (111). On the other hand, the surface of the silicon layer 107 exposed in the aperture 105 is a field (111).
[0083]According to the stencil mask of this embodiment, the aperture 105 is formed in consideration of the crystal face orientation of membrane material. The angle of the field which is the surface of the silicon layer 106 (110), and the field which is sections of the silicon layer 107 (111) to make is 54.7 degrees, and the field which is a section of the silicon layer 106 (111) is processed almost vertically to a mask surface.
[0084]Thus, since the tapered angle of the aperture 105 is controlled using the crystal face orientation of membrane material, a tapered angle can be made regularity also when minuteness making of the pattern is carried out further. Line width W_2 of a mask pattern is determined by thickness [of line width W_1 of silicon nitride film 108 portion, and the silicon layer 107] d, and the tapered angle.
[0085]If the resist of line width W_1 can be formed also when resist of line width W_2 cannot be formed on the silicon nitride film 108 according to the mask of this embodiment shown in drawing 8, A mask pattern can be formed by line width W_2 reduced rather than line width W_1. Here, since the tapered angle of an aperture is constant, line width W_1 is reduced with high precision.
[0086]Next, the manufacturing method of the stencil mask of this embodiment is explained. First, in order to manufacture the stencil mask of this embodiment, as shown in drawing 9 (a) and (b), the SOI wafer 111 and the multilayer silicon wafer 112 are pasted together, and the wafer 115 is formed. The SOI wafer 111 side is a field (110), and the multilayer silicon wafer 112 side of the lamination side at this time is a field (100).
[0087]The SOI wafer 111 has the silicon layer 106 via the silicon oxide 109 on the silicon wafer 102. The thickness of the silicon wafer 102 is 725 micrometers. The thickness of the silicon oxide 109 is 100 nm. The thickness of the silicon layer 106 is 100 nm. The surface of the silicon layer 106 is a field (110).
[0088]The multilayer silicon wafer 112 has the silicon layer 107 via the porous silicon layer 114 on the silicon wafer 113. The thickness of the silicon wafer 113 is 725 micrometers. The thickness of the porous silicon layer 114 is 300 nm. The thickness of the silicon layer 107 is 50 nm. The surface of the silicon layer 107 is a field (100).
[0089]The thickness of the silicon layer 106 of the SOI wafer 111 is suitably changed according to the energy of the electron beam at the time of performing EPL using a stencil mask. When the accelerating voltage of an electron beam is 2keV, it is desirable to make

thickness of the silicon layer 106 into the range of about 100-200 nm.

[0090]The porous silicon layer 114 of the multilayer silicon wafer 112 forms by performing anodization to the silicon wafer 113 in a fluoric acid solution. Specifically, current is sent by using the single crystal silicon wafer 113 as the anode in the solution containing fluoric acid and ethanol. Thereby, the micropore of the diameter of several nanometers is formed in the surface of the silicon wafer 113. A porous structure is controlled by specific resistance of the concentration of a solution, current density, or silicon. The thickness of the porous silicon layer 114 is determined according to time to send current. After porosity-izing the surface of the silicon wafer 113 by anodization, the silicon layer 107 is formed by epitaxial growth.

[0091]Then, the SOI wafer 111 and the multilayer silicon wafer 112 are pasted together. In order to paste a wafer together, after washing each wafer, the surface is contacted at a room temperature and it is made to join together according to Van der Waals force. Then, heat-treat, a covalent bond is made to form and lamination is strengthened.

[0092]The silicon oxide 109 of the SOI wafer 111 and the porous silicon layer 114 of the multilayer silicon wafer 112 are used as an etching stopper layer so that it may mention later. Therefore, if the crystallinity of the silicon layer 107 does not fall, changing into other materials is also possible.

[0093]Next, as shown in drawing 10 (c), the surface silicon wafer 113 and the porous silicon layer 114 of the wafer 115 are removed. After performing surface grinding until the porous silicon layer 114 is exposed from the surface of the wafer 115 in order to remove these layers, etching removes the porous silicon layer 114 selectively.

[0094]This etching can be performed at a room temperature, using the mixed liquor of fluoric acid and nitric acid as an etching reagent. As compared with single crystal silicon, the etch rate of porous silicon is remarkably quick, and it is also possible to make etch selectivity of porous silicon to single crystal silicon about into 100,000. Therefore, without doing damage to the silicon layer 107 of a ground, it can be accepted porous silicon layer 114 and can remove. The silicon layers 106 and 107 from which a crystal face differs mutually on the silicon wafer 102 are laminated by the above process.

[0095]Next, as shown in drawing 10 (d), the silicon nitride film 108 is formed as membrane supporters on the field (100) of the silicon layer 107. The silicon nitride film 108 is formed by CVD. The thickness of the silicon nitride film 108 shall be 500 nm.

[0096]If membrane supporters are the material which is not etched by etchant at the time of etching into the silicon layers 106 and 107, and can support the membrane of the size (for example, 25 mm squares) corresponding to a chip area, they can also change into other materials. When using KOH or TMAH as the silicon layer 106 and etchant for 107, silicon oxide can also be used instead of a silicon nitride film. If it is a range which can support a membrane, membrane supporters' thickness can also be changed. For example, a silicon nitride film or

silicon oxide may be formed by a thickness of about 400-800 nm as membrane supporters.
[0097]Next, as shown in drawing 10 (e), the rear-face side silicon oxide 116 is formed in the rear face of the wafer 115, and the resist 117 is formed in the surface by the pattern of a strut. As it mentioned above in Embodiment 1, when forming the strut 104 by dry etching, before etching is completed, resist may disappear. In order to prevent this, before forming resist by the pattern of a strut, the rear-face side silicon oxide 116 may be formed beforehand.
[0098]After etching into the rear-face side silicon oxide 116 by using resist 117 as a mask, as shown in drawing 11 (f), the resist 117 is removed if needed. Or it can also etch into the silicon wafer 102, with the resist 117 left.
[0099]Next, as shown in drawing 11 (g), it etches into the silicon wafer 102 by using the rear-face side silicon oxide 116 (resist 117 when [Or] the resist 117 remains) as a mask. Thereby, the strut 104 is formed. In this etching, the silicon oxide 109 serves as an etching stopper layer. In the case of the mask for LEEPL of an actual size projection system, the membrane field shown by an arrow is equivalent to a chip area.
[0100]Let this etching be the dry etching which used fluorine system gas, such as SF_6 and NF_3, for example, and the wet etching using KOH etc. If the strut 104 is formed by wet etching when the silicon wafer 102 surface of the SOI wafer 111 is a field (110), the section of the strut 104 turns into a field (111), and a strut section can be processed vertically.
[0101]Next, as shown in drawing 11 (h), the resist 118 is formed on the silicon nitride film 108. Interval W_1 of the resist 118 is made larger than line width W_2 of the silicon layer 106 shown in drawing 8. Then, the pattern of the resist 118 is transferred by the silicon nitride film 108 by etching into the silicon nitride film 108 by using resist 118 as a mask. Let this etching be the dry etching which used CF_4 etc., for example. Then, the resist 118 is removed as shown in drawing 12 (i).
[0102]Next, as shown in drawing 12 (j), wet etching is performed to the silicon layer 107 by using the silicon nitride film 108 as a mask. For example, when a wafer is immersed in a KOH solution with a temperature of 70 ** concentration 30wt%, the etching rate of field (111) silicon has an etching rate of field (100) silicon extremely as late as a part for 5-nm/to 797-nm being a part for /.
[0103]That is, in the perpendicular direction of the silicon layer 107, etching hardly advances with about 108 silicon nitride film to etching advancing promptly. Therefore, the etching section in the silicon layer 107 serves as tapered shape equivalent to a field (111), and this (111) field makes the angle of 54.7 degrees to the field (100) of the silicon layer 107 (refer to drawing 8).
[0104]As a result, line width W_2 of the silicon layer 107 in the interface of the silicon layer 106 and the silicon layer 107 becomes narrower than line width W_1 of the resist 118 or the silicon

nitride film 108. When thickness of the silicon layer 107 is set to d, it is expressed $W_2=W_1-2$ d/tan54.7" and line width W_1 is reduced to line width W_2 according to thickness d of the silicon layer 107. In this embodiment, a W_2=35nm detailed pattern is formed with high precision from thickness d of the silicon layer 107 being 50 nm by line width W_1 of the resist 118 or the silicon nitride film 108 being 105.8 nm, for example.

[0105]Then, the wafer 115 is immersed in a KOH solution, and as shown in drawing 12 (k), wet etching is performed to the silicon layer 106. It is extraordinarily [to the etching rate of the field which is an etching section of the silicon layer 107 (111) being a part for 5 nm// the etching rate of the field (110) of the silicon layer 106 surface / as a part for 1455 nm/] quick. Therefore, the field (110) of the silicon layer 106 is etched selectively.

[0106]About the aperture 105 of silicon layer 106 portion, since aperture 105 wall surface turns into a field (111), etching to a horizontal direction hardly advances. Thereby, the vertical sectional shape of the aperture 105 is acquired in silicon layer 106 portion. When an aperture is formed as mentioned above using the difference in the etching rate by a crystal face, sectional shape of an aperture can be made flat to an atomic layer order, or an aperture can be processed with vertical sectional shape.

[0107]Even if it uses a TMAH solution for etchant when performing wet etching to the silicon layers 107 and 106, an etching rate changes according to a crystal face. For example, when a wafer is immersed in a TMAH solution with a temperature of 80 ** concentration 20wt%, the etching rate of silicon becomes in respect of a part (110) for 603-nm/, and becomes a part for 17-nm/in a field (111) by 1114-nm/in a field (100). Therefore, like the case where a KOH solution is used, it can etch into a specific crystal face selectively, and the surface smoothness and shape of an aperture section can be controlled with high precision.

[0108]As shown in drawing 12 (k), after etching into the silicon layer 106, the silicon oxide 109 of membrane 103 portion is removed. The silicon oxide 109 is removable by the wet etching which used fluoric acid, for example. By the above process, the stencil mask 141 shown in drawing 7 is obtained.

[0109]Although not illustrated, before pasting together the SOI wafer 111 and the multilayer silicon wafer 112, after oxidizing the surface of at least one wafer, wafers may be pasted together in the manufacturing method of the mask of this above-mentioned embodiment. In that case, etching of silicon oxide is added between the etching process of the silicon layer 107, and the etching process of the silicon layer 106.

[0110]The manufacturing method of the semiconductor device of this embodiment includes the process of producing a stencil mask in accordance with the manufacturing method of the mask of this above-mentioned embodiment, and performing LEEPL using the produced mask. Since a minute pattern performs EPL using the mask formed with high precision according to the

manufacturing method of the semiconductor device of this embodiment, the pattern defect of an LSI pattern can be reduced.

[0111](Embodiment 4) Although line width W_2 narrower than interval W_1 of the resist 118 (refer to drawing 11 (h)) is obtained by forming the silicon layer 107 in the stencil mask 141 of Embodiment 3, When a direct and detailed pattern can be formed in resist, it is not necessary to form the silicon layer 107.

[0112]Drawing 13 is a sectional view of the mask of this embodiment, and drawing 14 is the figure to which the aperture part of drawing 13 was expanded. As shown in drawing 13, the stencil mask 151 of this embodiment has a stencil mask of Embodiment 3, and a common structure except for the silicon layer 107 not being formed.

[0113]As shown in drawing 14, in the interface of the silicon layer 106 and the silicon nitride film 108, the surface of the silicon layer 106 is a field (110). The surface of the silicon layer 106 exposed in the aperture 105 turns into a field (111) by this, and the aperture 105 is processed almost vertically to a mask surface. That is, the conversion difference of the resist used as the etching mask of the silicon nitride film 108 and line width W_3 of the silicon layer 106 is very small.

[0114]When manufacturing the stencil mask 151 of this embodiment, the lamination of a wafer is unnecessary, and as shown in drawing 15 (a), the silicon nitride film 108 is first formed on the SOI wafer 111. The SOI wafer 111 has the silicon layer 106 via the silicon oxide 109 on the silicon wafer 102 like Embodiment 3. The silicon nitride film 108 may be changed into silicon oxide etc.

[0115]Next, as shown in drawing 15 (b), the rear-face side silicon oxide 116 is formed by the pattern of a strut. Then, it etches into the silicon wafer 102 and the strut 104 is formed. Then, as shown in drawing 15 (c), dry etching is performed to the silicon nitride film 108, and a part of aperture 105 is formed.

[0116]Next, as shown in drawing 15 (d), wet etching which used KOH or a TMAH solution for the silicon layer 106 is performed, and the aperture 105 is formed. Then, the stencil mask 151 shown in drawing 13 is obtained by removing the silicon oxide 109 of membrane 103 portion.

[0117](Embodiment 5) Although the silicon nitride film 108 is formed in the stencil mask 141 of Embodiment 3 shown in drawing 7 as membrane supporters, even if it does not form membrane supporters, when the intensity of the membrane 103 is fully obtained, it is not necessary to form membrane supporters.

[0118]Drawing 16 and drawing 17 are the sectional views of the stencil mask of this embodiment. The stencil mask 161 of drawing 16 removes the silicon nitride film 108 from the stencil mask 141 of Embodiment 3. The stencil mask 171 of drawing 17 removes the silicon nitride film 108 from the stencil mask 151 of Embodiment 4.

[0119]When manufacturing these stencil masks 161 and 171, without forming membrane

supporters like a silicon nitride film, for example, resist is formed on the silicon layer 106 or the silicon layer 107, and it etches into the silicon layers 106 and 107 by using resist as a mask. Or where membrane supporters are laminated, an aperture is formed in the silicon layers 106 and 107, and membrane supporters are removed before using a stencil mask for lithography after that.

[0120]According to a mask of the embodiment of above-mentioned this invention, and a manufacturing method for the same, it becomes possible to form a detailed mask pattern with high precision. According to the manufacturing method of the semiconductor device of the embodiment of this invention, it becomes possible to transfer a detailed pattern with high precision in EPL.

[0121]The embodiment of a mask of this invention, and the manufacturing method and the manufacturing method of a semiconductor device for the same is not limited to the above-mentioned explanation. For example, the manufacturing method of the mask of this invention is also applicable to manufacture of other masks, such as stencil masks for EPL other than LEEPL(s), such as PREVAIL, a mask for good conversion type type electron beam direct writing machines or a mask for ion beam lithography, and a mask for X-ray lithography. Or it is also possible to apply the mask of this invention to the process of irradiating with charged particles, such as an ion implantation, locally, for example in addition to lithography. In addition, it is a range which does not deviate from the gist of this invention, and various change is possible.

[0122]

[Effect of the Invention]According to the mask of this invention, the sectional shape of an aperture and the surface smoothness of a section are controlled with high precision, and a detailed mask pattern is formed with high precision. According to the manufacturing method of the mask of this invention, it becomes possible to form a minute pattern in the mask for lithography with high precision. According to the manufacturing method of the semiconductor device of this invention, it becomes possible to transfer a minute pattern with high precision in a lithography process.

[Translation done.]